IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND the claims in accordance with the following:

1. (cancelled)

2. (currently amended) ~~The branch predicting device according to claim 1~~A branch predicting device, comprising:

a storing circuit storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, wherein

the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, wherein said storing circuit stores a register number of a link register, which is specified by the instruction equivalent to the subroutine call, as the information specifying the return address and wherein said storing circuit stores the return address of the subroutine as the information specifying the return address.

3. (cancelled)

4. (currently amended) A branch predicting device, comprising:

a stack circuit storing information specifying a return address of a subroutine;

a push circuit pushing the information specifying the return address onto said stack circuit, when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in a top entry of said stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, and wherein only the taken instruction of a branch instruction is thus registered.

5. (cancelled)

6. (currently amended) A branch predicting device, comprising:

a stack circuit storing information specifying a return address of a subroutine;

a push circuit pushing the information specifying the return address onto said stack circuit, when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in a top entry of said stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, and ~~The branch predicting device according to claim 5, wherein~~ said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine

return as the instruction equivalent to the subroutine return regardless of the result of the comparison, if the register number of the branch destination address register corresponds to a particular register commonly designated as the branch destination address register, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared.

7. (currently amended) A branch predicting device, comprising:

a stack circuit storing information specifying a return address of a subroutine;

a push circuit pushing the information specifying the return address onto said stack circuit, when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in a top entry of said stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison,

~~The branch predicting device according to claim 5,~~ wherein said push circuit does not push the register number of the link register onto said stack circuit if the register number of the link register corresponds to a particular register commonly designated as the branch destination address register, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared.

8. (original) The branch predicting device according to claim 4, further comprising

a pop circuit popping said stack circuit when said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine return as the instruction equivalent to the subroutine return, and a branch by the instruction equivalent to the subroutine return is taken.

9. (original) The branch predicting device according to claim 1, further comprising

a predicting circuit storing branch history information for a branch prediction, wherein

said comparing circuit makes the comparison between the information specifying the branch destination address and the information specifying the return address, when the branch history information is registered to said predicting circuit.

10. (currently amended) A branch predicting device, comprising:

a storing circuit storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected;

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison; and ~~The branch predicting device according to claim 1, further comprising~~

a circuit invalidating the information stored in said storing circuit when an event which causes a correspondence between a subroutine call and a subroutine return to be improper, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared.

11. (currently amended) The branch predicting device according to claim ~~1,~~ 2, further comprising:

a predicting circuit storing branch history information for a branch prediction; and

a setting circuit setting in said predicting circuit a flag indicating that a return destination of a detected instruction equivalent to a subroutine return differs, when an instruction equivalent to a subroutine return, which does not return to an instruction address immediately succeeding the instruction equivalent to the subroutine call, is detected.

12. (original) The branch predicting device according to claim 11, wherein said predicting circuit comprises a return address stack circuit storing the return address of the subroutine, pops said return address stack circuit if the flag is recognized at the time of a branch prediction, and does not use a popped return address as a predicted branch destination.

13. (currently amended) A branch predicting device, comprising:

a storing circuit storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison,

~~The branch predicting device according to claim 1, further comprising:~~

a predicting circuit storing branch history information for a branch prediction; ~~and~~

a circuit performing a control such that a predetermined flag is set when an instruction equivalent to a subroutine call, which is unregistered in the branch history of ~~to~~ said predicting circuit, is detected, the predetermined flag is reset when an instruction equivalent to a subroutine return, which corresponds to the unregistered instruction equivalent to the subroutine call, is detected, and the instruction equivalent to the subroutine return corresponding to the unregistered instruction is not identified as an instruction equivalent to a subroutine return in said predicting circuit,

the predicting circuit predicting the branch responsive to the identifying and the control, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared.

14. (currently amended) A branch predicting device, comprising:

a return address stack circuit storing a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return, and the return address stored in said return address stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, and wherein only the taken instruction of a branch instruction is thus registered.

15. (currently amended) A branch predicting method, comprising:

registering information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the registered information specifying the return address, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected;

identifying the instruction which can possibly be the instruction equivalent to the subroutine return as an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, if the information specifying the branch destination address and the information specifying the return address match;

identifying the instruction which can possibly be the instruction equivalent to the subroutine return not as the instruction equivalent to the subroutine return, which corresponds to the instruction equivalent to the subroutine call, if the information specifying the branch destination address and the information specifying the return address do not match; and

making a branch prediction by using an identification result, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, and wherein only the taken instruction of a branch instruction is thus registered.

16. (currently amended) A branch predicting device, comprising:

storing means for storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

comparing means for making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing means, and for outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

identifying means for identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, and wherein only the taken instruction of a branch instruction is thus registered.

17. (currently amended) A branch predicting device, comprising:

stack means for storing information specifying a return address of a subroutine;

push means for pushing the information specifying the return address onto said stack means, when an instruction equivalent to a subroutine call is detected;

comparing means for making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in a top entry of said stack means, and for outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

identifying means for identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, and wherein only the taken instruction of a branch instruction is thus registered.

18. (currently amended) A branch predicting device, comprising:

return address stack means for storing a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

comparing means for making a comparison between a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return, and the return address stored in said return address stack means, and for outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

identifying means for identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared, and wherein only the taken instruction of a branch instruction is thus registered.

19. (new) A branch predicting device, comprising:

a storing circuit storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

a comparing circuit comparing information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing circuit, and outputting a comparison result, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an determining circuit determining whether instruction equivalent to a subroutine call is an non-history instruction that does not get recorded in a branch history and determining whether the instruction which can possibly be an instruction equivalent to a subroutine return corresponds to the non-history instruction and outputting a determination result, when the

instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

a predicting circuit predicting the branch responsive to the comparison result and the determination result, and

wherein the predicted branch is the branch of the instruction equivalent to the subroutine return in an architecture for which a particular instruction for a subroutine is not prepared.